PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of	Docket No: Q53743
Takumi HASEGAWA	
Appln. No.: 09/273,560	Group Art Unit: 2123
Confirmation No.: 7269	Examiner: Kandasamy THANGAVELU
Filed: March 22, 1999	
For: DELAY ANALYSIS SYSTEM	

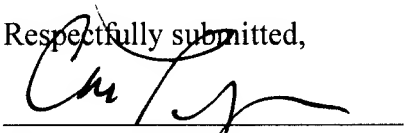
SUBMISSION OF APPEAL BRIEF

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith please find an Appeal Brief. The USPTO is directed and authorized to charge the statutory fee of $510 and all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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APPEAL BRIEF UNDER 37 C.F.R. § 41.37

MAIL STOP APPEAL BRIEF - PATENTS
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Sir:

In accordance with the provisions of 37 C.F.R. § 41.37, Appellant submits the following:

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I. REAL PARTY IN INTEREST

The real party in interest in this appeal is NEC CORPORATION. Assignment of the application was submitted to the U.S. Patent and Trademark Office on March 22, 1999, and recorded on the same date at Reel 9844, Frame 0659.

II. RELATED APPEALS AND INTERFERENCES

There are no known appeals or interferences that will affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-4 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over *Blinne et al.* (U.S. Patent No. 5,274,568) in view of *Hasegawa* (U.S. Patent No. 6,041,168) (hereinafter *Hasegawa '168*) and in further view of *Hasegawa* (U.S. Patent No. 5,528,511) (hereinafter *Hasegawa '511*).

The rejections of claims 1-4 are being appealed.

IV. STATUS OF AMENDMENTS

An amendment after the Final Office Action was filed on May 2, 2007. In the Advisory Action dated May 24, 2007, the Examiner stated that the amendment would be entered for purposes of appeal. The claims in the Appendix are the amended claims filed on May 2, 2007.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The claimed invention relates to a system for analyzing a delay in a logic circuit device, and more particularly to a library for delay analysis. Specification, page 1, lines 5-7.

When calculating a delay in a logic circuit in conventional delay simulation systems, a delay analysis library containing circuit connection information and delay information on the basic elements (such as AND elements) of the circuit is used. The delay analysis library contains connection information as well as delay information which is composed of the delay time of each rise and fall. But, it does not contain logic information on the circuit. For this reason, the circuit delay analysis uses the worst delay times stored in the delay analysis library, sometimes preventing the delay analysis from being made correctly. Specification, page 1, lines 9-21.

In view of the foregoing, an objective of the claimed invention to provide a delay analysis system and a delay analysis method for analyzing delays and calculating delay times considering circuit logic information. To achieve this objective, the delay analysis library contains not only connection information on a plurality of circuits and delay time information on the rises and falls of the input and output terminals, but also logic information on the logic operation of the plurality of circuits. When making the delay analysis of a logic circuit, the system selects a delay time information according to the logic operation of the circuits included in the logic circuit, the delay time being between the input terminals and output terminals of the circuits, from the library which contains the delay time information on the rises and falls of the input terminals and output terminals. Specification, page 2, line 17 to page 3, line 9.

In the claimed invention, the delay time is determined by comparing the input signal at a first point and the propagated signal (signal at a subsequent circuit point after propagation) at the second point. For example, assume that the data signal of a first flip-flop is "rising edge" at the first time point when a clock signal is input. Then, at the time point when the next clock signal is received, the question is whether or not the propagated signal at the next flip-flop is propagated as "rising edge" (in other words, whether the next trigger of the clock signal can occur in association with the rising edge of the propagated signal).

Figure 3, for example, represents the logical consequence of an AND gate (two inputs 1 and 2, and output 3) of figure 2. Assume the case where the state changes LOW-HIGH-LOW within a period of two clock signals. At the time in which the second clock signal is input, the state is "LOW," which is regarded to be the same state as the first signal state. Thus, there is no recognition of "rising" (LOW-HIGH) in view of the operation per clock unit. Therefore, the case where the delay is "NONE" (at the column Rise/Fall), will not indicate any change in the signal state (between LOW and HIGH) which means that there is no need to make a target (object) of the timing analysis for the case "NONE" in figure 3. In the claimed invention, the situation where there is no change in signal state (i.e., a nullified state) is determined automatically as a result of the logic AND circuit. See specification at page 5, line 2 through page 6, line 11.

The subject matter of each of the independent claims, with reference to the specification, is identified below.

1. A delay analysis system for making a delay analysis of a logic circuit,

said system having a delay analysis library (figure 1) comprising connection information (figure 1a) and delay time information (figure 1b) for a plurality of circuits (Page 5, line 20 to Page 6, line 18),

wherein, for at least one circuit of said plurality of circuits, said library further comprises logical operation information (figure 1c), wherein delay time information is provided for a signal path from input terminals to output terminals of a logical circuit (figure 2) and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal, and wherein said delay time information for each signal path of the logical circuit of said at least one circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at said output terminals corresponding to logical operation information (Page 6, line 23 to page 8, line 9).

2. A delay analysis system for making a delay analysis of a logic circuit,

said system having a delay analysis library (figure 1) comprising connection information (figure 1a) and delay time information (figure 1b) for a plurality of circuits (Page 5, line 20 to Page 6, line 18),

wherein, for each of said plurality of circuits, said library further comprises logical operation information (figure 1c), wherein delay time information is provided for a signal path from input terminals to output terminals of a logical circuit (figure 2) and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal for each circuit of said plurality of circuits, and wherein said delay time information for each signal path of said plurality of circuits is based upon logical state

transitions at said input terminals and corresponding logical state transitions at said output terminals corresponding to logical operation information for said plurality of circuits. (Page 6, line 23 to page 8, line 9).

3. A method for making a delay analysis of a logic circuit, comprising:

referencing a delay analysis library (figure 1) for a plurality of circuits, said delay analysis library comprising connection information (figure 1a), delay time information (figure 1b) and logic operation information (figure 1c), wherein delay time information is provided for a signal path from input terminals of a logical circuit (figure 2) and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of said plurality of circuits, said delay time information for each signal path of said at least one circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at each output terminal as represented by logical operation information for said at least one circuit (Page 6, line 23 to page 8, line 9); and

if the logic circuit comprises said at least one circuit, selecting a delay time of each path of said at least one circuit from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on the input terminal whose logical transition triggers said low state to high state transition of said selected output terminal according to the logical operation information, or if a selected output terminal transitions from a high state to a low state, said delay time is selected based on the input terminal

whose logical transition triggers said high state to low state transition of said selected output terminal according to the logical operation information (Page 6, line 23 to page 8, line 9)..

4. A computer-readable medium having stored thereon a program comprising computer instructions that, when executed on a computer, perform a process for executing a delay analysis method for a logic circuit, said computer-readable medium causing a computer to execute said method, wherein said method comprises:

referencing a delay analysis library for a plurality of circuits (figure 1), said delay analysis library comprising connection information (figure 1a), delay time information (figure 1b) and logic operation information (figure 1c), wherein delay time information is provided for a signal path from input terminals of a logical circuit (figure 2) and wherein a delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of said plurality of circuits, said delay time information for each signal path of said at least one circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at each output terminal as represented by logical operation information for said at least one circuit (Page 6, line 23 to page 8, line 9);

if said logic circuit comprises said at least one circuit, selecting a delay time of each path of said at least one circuit from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on the input terminal whose logical transition triggers said low state to high state transition of said selected output

terminal according to the logical operation information, or if a selected output terminal transitions from a high state to a low state, said delay time is selected based on the input terminal whose logical transition triggers said high state to low state transition of said selected output terminal according to the logical operation information (Page 6, line 23 to page 8, line 9); and

performing a delay calculation to determine a propagation delay time using said selected delay time of said at least one circuit (Page 6, line 23 to page 8, line 9).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellant requests that the following rejections be reviewed:

1. The rejection of claims 1-4 under 35 U.S.C. § 103(a) as being unpatentable over *Blinne et al.* (U.S. Patent No. 5,274,568) in view of *Hasegawa* (U.S. Patent No. 6,041,168) (hereinafter *Hasegawa '168*) and in further view of *Hasegawa* (U.S. Patent No. 5,528,511) (hereinafter *Hasegawa '511*).

No other grounds of rejection or objection currently are pending.

This appeal is directed to claims 1-4.

VII. ARGUMENT

1. The rejections of claims 1-4 under 35 U.S.C. § 103(a) as allegedly being unpatentable over *Blinne et al.* in view of *Hasegawa '168* and in further view of *Hasegawa '511*).

Appellant respectfully requests the members of the Board to reverse the aforementioned rejections of claims 1-4 under 35 U.S.C. § 103(a) as allegedly being unpatentable over *Blinne et al.* in view of *Hasegawa '168* and in further view of *Hasegawa '511*). Appellant disagrees with the Examiner's rejections because the cited references fails to disclose or suggest all of the claim limitations.

Claims 1-4 require, among other limitations, wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal. The Examiner acknowledges that the combination of *Blinne* and *Hasegawa '168* fails to teach or suggest the claim element above (FOA pages 3-4). The Examiner asserts that Hasegawa '511 teaches this required claim element (FOA pages 4; Examiner *citing to Hasegawa '511* at Fig. 3; col. 1, lines 28-35; col. 2, lines 30-42; and col. 3, lines 5-26). Appellant respectfully disagrees.

Hasegawa '511 at Fig 3 shows a timing diagram for two inputs and an output of an OR device (col. 4, lines 43-45; col. 1, lines 28 -35). As shown in Fig. 3, there is a 1 ns delay from node p to node s due to interim device 230 (Figs. 2, 3, and 4). In contrast, node p to node v has no delay, 0 ns, because it is a short circuit. (Figs. 2, 3, and 4). Likewise, transmission from node r to node s (path c) has no delay as this path is also a short circuit (Fig. 12). Also a transition, an R (rise) or an F (fall) is not a valid condition for path c, because it is a short circuit. Therefore,

nodes r and s must be the same logic, hi or lo (col. 3, lines 17-27). At time equals 0 ns, the output terminal goes high as there is a difference in states at its input terminals, nodes s and v (Fig. 3) and the output terminal goes high without delay. According to the timing diagram of Fig. 3 at time equals (from) 1 ns to 2 ns, the output terminal is high. However, this is counter-intuitive, given that no delay is taught for transmission from nodes s and v to node t, and that node s (path 250) rises to hi at 1 ns becoming the logic state equal to node v, the other input on an OR gate. Therefore, intuitively, one ordinarily skilled would expect the output terminal to fall to lo from 1 ns to 2 ns and then rise hi again as node v falls to lo.

Hasegawa '511 specifically teaches 0 ns delay for path f to g (col. 2, lines 34-35) and a 1 ns delay for path a to b to c to d (Figs 2, 3, and 4). Path d is the path from one input terminal of the OR gate to the output terminal of the same and path g is the other input to output path of the OR gate. This 1 ns delay is attributed to device 230 (col. 1, lines 20-23) and is not attributed to the OR gate or the path d.

Hasegawa '511 teaches delay time verifying, wherein rise and fall are not permitted between nodes connected by a short circuit (col. 3, lines 3-26). *Hasegawa '511* teaches 0 ns delay for path d and path g, the two input to one output paths of the OR gate. *Hasegawa '511* confusingly teaches an OR gate which fails to respond to two simultaneously hi inputs (Fig. 3). *Hasegawa '511* teaches that input to output paths in a given OR gate are equal with respect to delay. *Hasegawa '511* fails to teach delay time information that is specific to an input terminal logical state transition and resulting logical state transition at an output terminal, as taught by the subject application and required by the claims (Fig. 5-7; claims 1-4). *Blinne*, *Hasegawa '168,*

and *Hasegawa* '511, fail to teach or suggest, either alone or in combination, delay time information that is specific to an input terminal logical state transition and resulting logical state transition at an output terminal. At least for this deficiency, the rejection of claims 1-4 as being unpatentable over *Blinne* in view of *Hasegawa '168* and in further view of *Hasegawa '511* under 35 U.S.C. § 103(a), should be withdrawn.

In the claimed invention, the delay time is determined by comparing the input signal at a first point and the propagated signal (signal at a subsequent circuit point after propagation) at the second point. For example, assume that the data signal of a first flip-flop is "rising edge" at the first time point when a clock signal is input. Then, at the time point when the next clock signal is received, the question is whether or not the propagated signal at the next flip-flop is propagated as "rising edge" (in other words, whether the next trigger of the clock signal can occur in association with the rising edge of the propagated signal).

Figure 3, for example, represents the logical consequence of an AND gate (two inputs 1 and 2, and output 3) of figure 2. Assume the case where the state changes LOW-HIGH-LOW within a period of two clock signals. At the time in which the second clock signal is input, the state is "LOW," which is regarded to be the same state as the first signal state. Thus, there is no recognition of "rising" (LOW-HIGH) in view of the operation per clock unit. Therefore, the case where the delay is "NONE" (at the column Rise/Fall), will not indicate any change in the signal state (between LOW and HIGH) which means that there is no need to make a target (object) of the timing analysis for the case "NONE" in figure 3. In the claimed invention, the situation where there is no change in signal state (i.e., a nullified state) is determined

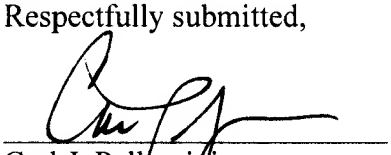
automatically as a result of the logic AND circuit. See specification at page 5, line 2 through page 6, line 11.

On the other hand, in Hasegawa '511, the occurrence of a "nullified state" must be identified explicitly.

Unless a check is submitted herewith for the fee required under 37 C.F.R. §41.37(a) and 1.17(c), please charge said fee to Deposit Account No. 19-4880.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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Date: October 2, 2007

CLAIMS APPENDIX

CLAIMS 1-4 ON APPEAL:

1. A delay analysis system for making a delay analysis of a logic circuit,

said system having a delay analysis library comprising connection information and delay time information for a plurality of circuits,

wherein, for at least one circuit of said plurality of circuits, said library further comprises logical operation information, wherein delay time information is provided for a signal path from input terminals to output terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal, and wherein said delay time information for each signal path of the logical circuit of said at least one circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at said output terminals corresponding to logical operation information.

2. A delay analysis system for making a delay analysis of a logic circuit, said system having a delay analysis library comprising connection information and delay time information for a plurality of circuits,

wherein, for each of said plurality of circuits, said library further comprises logical operation information, wherein delay time information is provided for a signal path from input terminals to output terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal

for each circuit of said plurality of circuits, and wherein said delay time information for each signal path of said plurality of circuits is based upon logical state transitions at said input terminals and corresponding logical state transitions at said output terminals corresponding to logical operation information for said plurality of circuits.

3. A method for making a delay analysis of a logic circuit, comprising:

referencing a delay analysis library for a plurality of circuits, said delay analysis library comprising connection information, delay time information and logic operation information, wherein delay time information is provided for a signal path from input terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of said plurality of circuits, said delay time information for each signal path of said at least one circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at each output terminal as represented by logical operation information for said at least one circuit; and

if the logic circuit comprises said at least one circuit, selecting a delay time of each path of said at least one circuit from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on the input terminal whose logical transition triggers said low state to high state transition of said selected output terminal according to the logical operation information, or if a selected output terminal transitions from a high state to a low state, said delay time is selected based on the input terminal

whose logical transition triggers said high state to low state transition of said selected output terminal according to the logical operation information.

4. A computer-readable medium having stored thereon a program comprising computer instructions that, when executed on a computer, perform a process for executing a delay analysis method for a logic circuit, said computer-readable medium causing a computer to execute said method, wherein said method comprises:

referencing a delay analysis library for a plurality of circuits, said delay analysis library comprising connection information, delay time information and logic operation information, wherein delay time information is provided for a signal path from input terminals of a logical circuit and wherein a delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of said plurality of circuits, said delay time information for each signal path of said at least one circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at each output terminal as represented by logical operation information for said at least one circuit;

if said logic circuit comprises said at least one circuit, selecting a delay time of each path of said at least one circuit from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on the input terminal whose logical transition triggers said low state to high state transition of said selected output terminal according to the logical operation information, or if a selected output terminal

transitions from a high state to a low state, said delay time is selected based on the input terminal whose logical transition triggers said high state to low state transition of said selected output terminal according to the logical operation information; and

performing a delay calculation to determine a propagation delay time using said selected delay time of said at least one circuit.

EVIDENCE APPENDIX:

This Section Is Not Applicable To The Instant Appeal.

RELATED PROCEEDINGS APPENDIX

This Section Is Not Applicable To The Instant Appeal.